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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,340	07/03/2003	Stephen L. Bass	10981292-2	5093

7590 07/13/2005

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/613,340	BASS ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 30-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 30-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 05/02/2005.

2. Claims 1-18 and 30-39 are pending in this application. Claims 1, 7, 13, and 32 are independent claims. In Amendment, claims 19-29 are cancelled and claim 39 is added. This Office Action is made final.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-18 and 30-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Taborn et al. (U.S. 5,550,767).

Re claim 1, Taborn et al. disclose in Figures 2 and 4 an exponent computation apparatus for performing either an overflow or underflow comparison while minimizing overflow/underflow comparison circuitry (e.g. abstract and col. 2 lines 15-24), apparatus comprising: overflow/underflow possible check circuitry (e.g. Figure 2 and 4 as output signal of 72 and col. 9 lines 34-41), overflow/underflow possible check circuitry configured to determine if a mathematical operation involving a first exponent signal and a second exponent signal (e.g. B and AC exponents) creates a potential overflow

condition (output of 80), overflow/underflow possible check circuitry is configured to generate a underflow/overflow signal indicating if overflow condition is a possibility (e.g. output of 80) and generate an exponent selection signal (e.g. output signal of 24 that goes into the mux 27 and underflow/overflow detector 10), and wherein exponent selection signal is indicative of first exponent signal if first exponent signal is greater than second exponent signal and is indicative of second exponent signal if second exponent signal is greater than first exponent signal (e.g. col. 1 lines 14-22, col. 4 lines 31-53); and exponent compare circuitry (e.g. 78-79), exponent compare circuitry configured to compute an actual overflow/underflow condition (e.g. 78-79) for first or second exponent signal based upon exponent selection signal (e.g. 10 in Figure 1), exponent compare circuitry configured to compute an actual overflow condition if underflow/overflow signal indicates overflow is possible (e.g. 79 with output of 80 as 72 enable), and exponent compare circuitry configured to computes an actual underflow condition if underflow/overflow signal does not indicate overflow is possible (e.g. 78 with output of 72 enable).

Re claim 2, Taborn et al. further disclose in Figures 1-4 an exponent compare circuitry generates an error signal if an actual overflow/underflow condition exists (col. 9 lines 41-48 and col. 9 lines 60-65).

Re claim 3, Taborn et al. further disclose in Figures 1-4 a pre-normalized exponent selection circuitry configured to determine a larger exponent between first exponent signal and second exponent signal (Figures 1 and 2).

Re claim 4, Taborn et al. further disclose in Figures 1-4 an overflow/underflow possible check circuitry uses largest exponent to determine if mathematical operation between first exponent signal and second exponent signal creates overflow condition (Figure 2 part 51 and col. 7 lines 61-68).

Re claim 5, Taborn et al. further disclose in Figures 1-4 an exponent shift amount circuitry configured to determine how much the mantissa of largest exponent must be shifted to be normalized, and configured to compute a normalized exponent (35 and 39 in Figure 1).

Re claim 6, Taborn et al. further disclose in Figures 1-4 an exponent compare circuitry uses normalized exponent to determine if mathematical operation between first exponent signal and second exponent signal creates overflow condition (Figure 2 part 51 and col. 7 lines 63-68 and col. 8 lines 1-9).

Re claim 7, it is a method claim of claim 1. Thus, claim 7 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 8, it is a method claim of claim 2. Thus, claim 8 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 9, it is a method claim of claim 3. Thus, claim 9 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 10, it is a method claim of claim 4. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 11, it is a method claim of claim 5. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 12, it is a method claim of claim 6. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 13, it is an apparatus claim of claim 1. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 14, it is an apparatus claim of claim 2. Thus, claim 14 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 15, it is an apparatus claim of claim 3. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 16, it is an apparatus claim of claim 4. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 17, it is an apparatus claim of claim 5. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 18, it is an apparatus claim of claim 6. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 30, Tahorn et al. further disclose in Figures 1-4 the exponent compare circuit is further configured to perform multiple simultaneous compares of an exponent and a plurality of overflow thresholds if signal indicates the possibility of an overflow (e.g. section of circuit for producing output of 65 and 66 in Figure 3).

Re claim 31, Tahorn et al. further disclose in Figures 1-4 the exponent compare circuit is further configured to perform multiple simultaneous compares of an exponent and a plurality of underflow thresholds if signal indicates the possibility of an underflow (e.g. section of circuit for producing output of 67 in Figure 3).

Re claim 32, Tahorn et al. disclose in Figures 1-7 a method for performing overflow and underflow comparisons with exponent comparison circuitry (abstract) comprising the steps of: selecting (e.g. Figure 6 part 100) an exponent precision underflow/overflow constant from a plurality of exponent underflow/overflow constants (e.g. the exponent shift value); generating a sum signal and a carry signal (e.g. output value of 39 or the final answer) from one of plurality of exponent underflow/overflow constants (e.g. output of 10), a pre-normalized exponent signal (e.g. output of 37) and a normalization shift amount signal (e.g. output of 35); computing an underflow/overflow result from sum signal and carry signal (e.g. 10 in Figure 1); and transmitting an underflow/overflow condition based upon underflow/overflow result and an exponent adjust amount signal (e.g. Figure 4).

Re claim 33, Tahorn et al. further disclose in Figures 1-7 the selecting steps further comprises selecting constants via a plurality of constant selectors (e.g. 100-105).

Re claim 34, Tahorn et al. further disclose in Figures 1-7 plurality of constant selectors comprises two constant selectors (e.g. 100 and 101).

Re claim 35, Tahorn et al. further disclose in Figures 1-4 the generating step further comprises generating sum signal and carry signal via a plurality of carry save adders (e.g. output of either 30 or 39 in Figure 1).

Re claim 36, Tahorn et al. further disclose in Figures 1-4 the computing step further comprises computing underflow/overflow result via a plurality of comparators (e.g. Figure 3 or 4).

Re claim 37, Tahorn et al. further disclose in Figures 1-7 plurality of comparators further comprises four comparators (e.g. 100-103) and wherein a first one of four comparators uses a least significant bit of carry signal (e.g. signal from decoder 77) from one of plurality of carry save adders and a carry-in signal (e.g. signal from adder 25 in Figure 1) to extent the range of constant being compared.

Re claim 38, Tahorn et al. further disclose in Figures 6-7 exponent compare circuitry comprises a plurality of underflow/overflow result selectors, each result selector configured to transmit overflow condition and underflow condition based upon an underflow/overflow result from a plurality of comparators and further based upon an exponent adjust amount signal (e.g. Figures 6 for underflow and 7 for overflow).

Re claim 39, Tahorn et al. further disclose in Figures 6-7 computation of portion of mathematical operation is performed via a carry save adder (e.g. 23 in Figure 1) and a comparator (e.g. Figures 2-5).

Response to Arguments

5. Applicant's arguments filed 05/02/2005 have been fully considered but they are not persuasive.

a. The applicant argues in pages 11-15 generally for claims 1-18 that the cited reference by Taborn et al. fails to disclose "a overflow/underflow possible check circuitry is configured to generate a signal indicating if overflow condition is a possibility and generate an exponent selection signal indicative of first exponent signal if first exponent signal is greater than second exponent signal or generate exponent selection signal

indicative of second exponent signal if second exponent signal is greater than first exponent signal" and the reference also fails to disclose "the exponent compare circuitry is configured to compute an actual overflow/underflow condition for first or second exponent signal based upon exponent selection signal," as cited in the claimed invention.

The examiner respectfully submits that these new limitations are added recently and are clearly rejected with citations as seen in the above rejection. To re-state, the cited reference clearly discloses a overflow/underflow possible check circuitry is configured to generate a signal indicating if overflow condition is a possibility (e.g. Figure 1 generally) and generate an exponent selection signal (e.g. output signal of 24 in Figure 1 which used to selectively mux either the exponent B or AC) indicative of first exponent signal if first exponent signal is greater than second exponent signal or generate exponent selection signal indicative of second exponent signal if second exponent signal is greater than first exponent signal (e.g. col. 1 lines 14-22, col. 4 lines 31-53) and the exponent compare circuitry is configured to compute an actual overflow/underflow condition for first or second exponent signal based upon exponent selection signal (e.g. 10 in Figure 1).

b. The applicant argues in page 15-16 for claim 32 that the cited reference by Taborn et al. fails to disclose an error signal is produced by generating a sum signal and a carry signal from one of plurality of exponent underflow/overflow constants, a pre-normalized exponent signal and a normalization shift amount signal and computing an underflow/overflow result from said sum signal and carry signal.

The examiner respectfully submits that the cited reference clearly shows the step of generating a sum signal and a carry signal (e.g. output of 23 in Figure 1) from one of plurality of exponent underflow/overflow constants (e.g. depending on the exponents of A, B, and C), a pre-normalized exponent signal and a normalization shift amount signal (e.g. output control signals from 24) and computing an underflow/overflow result from said sum signal and carry signal (e.g. output of 37 into 10 in Figure 1).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

c. U.S. Patent No. 5,257,216 to Sweedler discloses a floating-point safe instruction recognition apparatus.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

July 4, 2005

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